Dual P-channel enhancement mode MOS transistor

PHP225

FEATURES

- High speed switching
- No secondary breakdown
- Very low on-resistance.

APPLICATIONS

- Motor and actuator driver, power management, synchronized rectifying, etc.

PINNING - SO8 (SOT96-1)

PIN	SYMBOL	DESCRIPTION
1	s_1	source 1
2	g_1	gate 1
3	s_2	source 2
4	g_2	gate 2
5	d_2	drain 2
6	d_2	drain 2
7	d_1	drain 1
8	d_1	drain 1

DESCRIPTION

Two P-channel enhancement mode MOS transistors in an 8-pin plastic SO8 (SOT96-1) package.

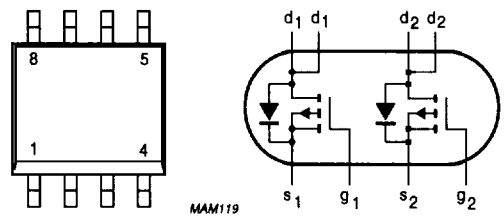

Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per P-channel					
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{SD}	source-drain diode forward voltage	I_S = –1.25 A	–	–1.6	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = –1 mA; V_{DS} = V_{GS}	–1	–2.8	V
I_D	drain current (DC)		–	–2.3	A
R_{DSon}	drain-source on-state resistance	I_D = –1 A; V_{GS} = –10 V	–	0.25	Ω
P_{tot}	total power dissipation	up to T_s = 80 °C;	–	2	W

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per P-channel					
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)	$T_s \leq 80$ °C	–	–2.3	A
I_{DM}	peak drain current	note 1	–	–10	A
P_{tot}	total power dissipation	up to $T_s = 80$ °C; note 2	–	2	W
		up to $T_{amb} = 25$ °C; note 3	–	2	W
		up to $T_{amb} = 25$ °C; note 4	–	1	W
		up to $T_{amb} = 25$ °C; note 5	–	1.3	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C
Source-drain diode					
I_S	source current (DC)	$T_s \leq 80$ °C	–	–1.25	A
I_{SM}	peak pulsed source current	note 1	–	–5	A

Notes

1. Pulse width and duty cycle limited by maximum junction temperature.
2. Maximum permissible dissipation per MOS transistor. (So both devices may be loaded up to 2 W at the same time).
3. Maximum permissible dissipation per MOS transistor. Value based on PCB with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Maximum permissible dissipation per MOS transistor. Value based on PCB with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.
5. Maximum permissible dissipation if only one MOS transistor dissipates. Value based on PCB with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

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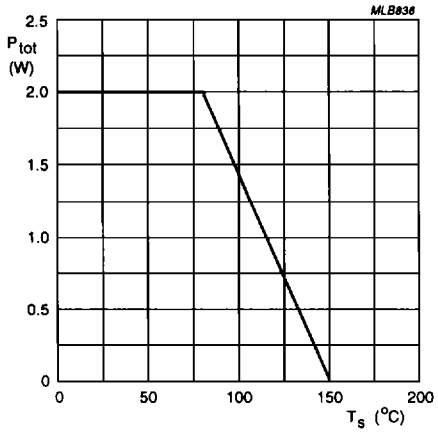
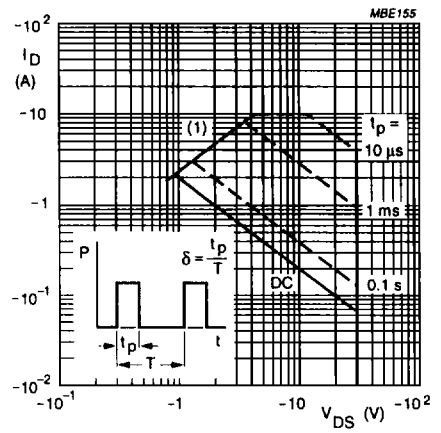


Fig.2 Power derating curve.



$\delta = 0.01$.
$T_s = 80$ °C.
(1) R_{DSon} limitation.

Fig.3 DC SOAR.

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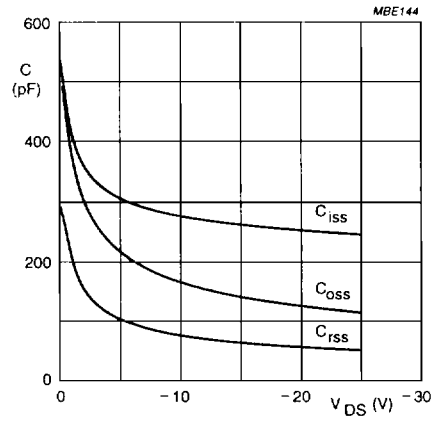
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	35	K/W

CHARACTERISTICS

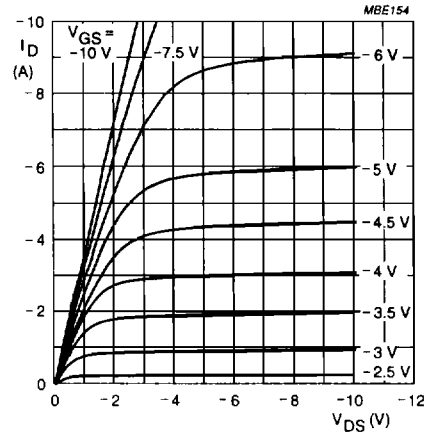
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per P-channel						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−1	–	−2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −24 V	–	–	−100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
I_{Don}	on-state drain current	V_{GS} = −10 V; V_{DS} = −1 V	−2.3	–	–	A
		V_{GS} = −4.5 V; V_{DS} = −5 V	−1	–	–	A
R_{DSon}	drain-source on-state resistance	V_{GS} = −4.5 V; I_D = −0.5 A	–	0.33	0.4	Ω
		V_{GS} = −10 V; I_D = −1 A	–	0.22	0.25	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{DS} = −20 V; I_D = −1 A	1	2	–	S
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −20 V; f = 1 MHz	–	250	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −20 V; f = 1 MHz	–	140	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −20 V; f = 1 MHz	–	50	–	pF
Q_g	total gate charge	V_{GS} = −10 V; V_{DS} = −15 V; I_D = −2.3 A	–	10	25	nC
Q_{gs}	gate-source charge	V_{GS} = −10 V; V_{DS} = −15 V; I_D = −2.3 A	–	1	–	nC
Q_{gd}	gate-drain charge	V_{GS} = −10 V; V_{DS} = −15 V; I_D = −2.3 A	–	3	–	nC
t_{on}	turn-on time	V_{GS} = 0 to −10 V; V_{DD} = −20 V; I_D = −1 A; R_L = 20 Ω	–	20	80	ns
t_{off}	turn-off time	V_{GS} = −10 to 0 V; V_{DD} = −20 V; I_D = −1 A; R_L = 20 Ω	–	50	140	ns
Source-drain diode						
V_{DS}	source drain diode forward voltage	V_{GS} = 0; I_S = −1.25 A	–	–	−1.6	V
t_{rr}	reverse recovery time	I_S = −1.25 A; di/dt = 100 A/μs	–	150	200	ns



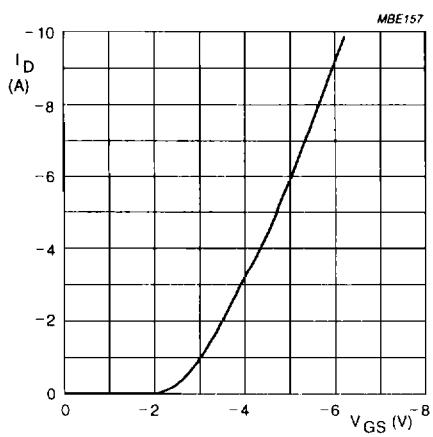
V_{GS} = 0.
T_j = 25 °C.

Fig.4 Capacitance as a function of drain-source voltage; typical values.



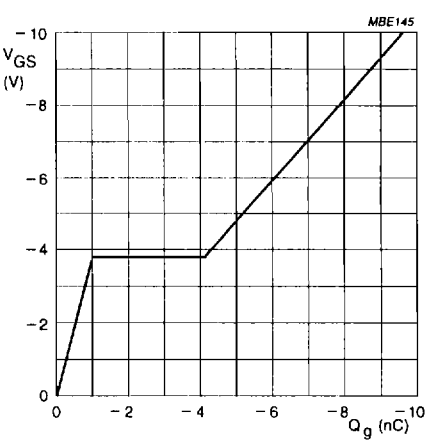
T_j = 25 °C.

Fig.5 Typical output characteristics.



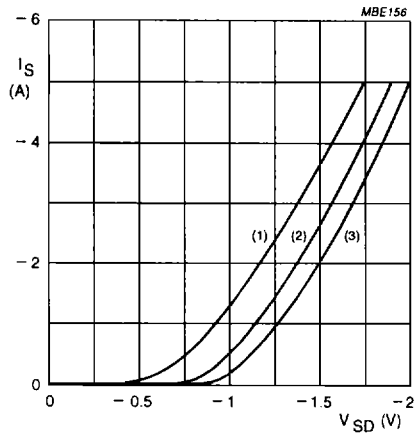
V_{DS} = −10 V.
T_j = 25 °C.

Fig.6 Typical transfer characteristics.



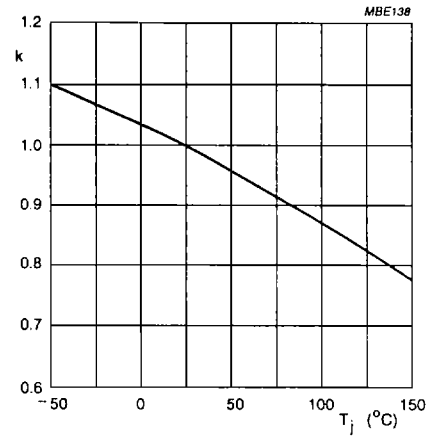
V_{DD} = −15 V.
I_D = −2.3 A.

Fig.7 Gate-source voltage as a function of total gate charge.



$V_{GD} = 0$.
(1) $T_j = 150$ °C.
(2) $T_j = 25$ °C.
(3) $T_j = -55$ °C.

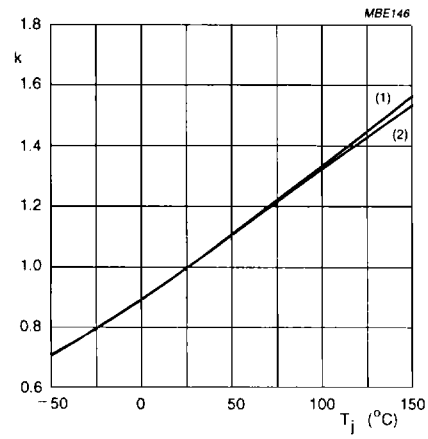
Fig.8 Source current as a function of source-drain diode forward voltage.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25\,°C}$$

Typical V_{GSth} at $I_D = 1$ mA; $V_{DS} = V_{GS} = V_{th}$.

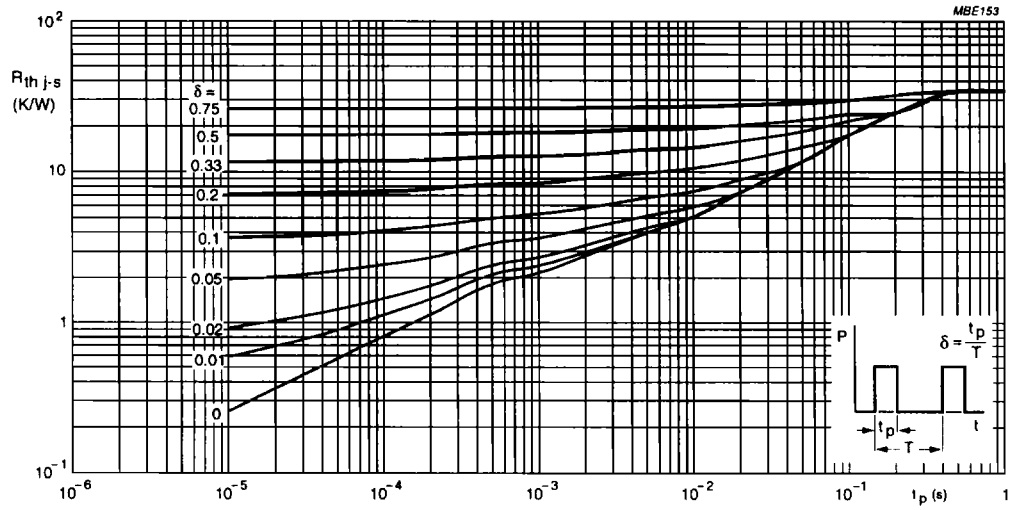
Fig.9 Temperature coefficient of gate-source threshold voltage.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\,°C}$$

Typical R_{DSon} at:
(1) $I_D = -1$ A; $V_{GS} = -10$ V.
(2) $I_D = -0.5$ A; $V_{GS} = -4.5$ V.

Fig.10 Temperature coefficient of drain-source on-resistance.



Solder point temperature T_s = 80 °C.

Fig.11 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.